REMARKS

This Amendment, submitted in response to the Office Action of October 3, 2000, is believed to be fully responsive to each point of rejection raised therein. Accordingly, favorable reconsideration on the merits is respectfully requested.

Claims 1-11 are pending in the application. The Examiner rejects claims 4-6, 10 and 11 under 35 U.S.C. §112, second paragraph, as being indefinite, and objects to claims 4-6 and 10-11 under 37 C.F.R §1.75 as being in improper form (i.e., improper multiple dependencies). Also, the Examiner rejects claims 1-3 and 7-9 under 35 U.S.C. §102(e) as being clearly anticipated by Nakai et al (Nakai). Finally, the Examiner indicates that claims 4-6, 10 and 11 have not been considered on the merits because of the improper multiple dependencies. Applicant hereinabove amends the claims to describe the invention more particularly and to obviate the objections to the claims. Applicant further respectfully submits the following arguments in traversal of the prior art rejections.

Applicant's invention is in the field of two-dimensional matrix type light modulation devices (such as flat displays and video projectors) and light emission devices (such as thin-film ELs, organic ELs, LEDs and FEDs), and provides two-dimensional matrix type light modulation and light emission devices comprising "a drive circuit constituted by ferroelectric gate field - effect transistors respectively connected to the pixel electrodes" (Applicant's specification, page 6, lines 13-15; and page 7, lines 24-27).

In particular, by arranging and driving ferroelectric gate field effect transistors as recited in claims 2, 4-6, 8, 10 and 11, Applicant's claimed invention reduces the number of transistors

required to drive light modulation and light emission devices (as compared to conventional devices), and allows to perform high-speed writing operations.

Turning to the cited art, Nakai relates to a drive circuit for a matrix of pixel electrodes. Claim 1 of Nakai recites a means for applying a first data signal (first signal line), a means for providing a second data signal (second signal line), a means for exclusively holding a selecting signal, and a selecting means for applying the first data signal or the second data signal to the first electrode in response to the selecting signal held in the holding means. In Nakai, a first switching element and a second switching element which turn on or off in a complementary way corresponding to a selecting signal held by the holding means and specifically the switching elements are the n-channel FET and the p-channel FET. Nakai requires selecting a ferromagnetic FET for a specific image pixel circuit in order to write data (for selecting one of the above two data signals) to the ferromagnetic FET of the specific image pixel circuit in the matrix. To this end, a normal FET (MOS-FET) is provided as the selecting circuit (element 101 in Fig.1, elements 501 and 502 in Fig. 5, element 501 in Fig. 6, and element 801 in Fig. 8). Therefore, in order to write data to the specific ferromagnetic FET in the matrix, Nakai selects a normal FET with the row signal (ex. element 102 of Fig. 1) and writes data to the ferromagnetic FET (elements 104 and 106 of Fig. 1) with the column signal (ex. element 103 of Fig. 1) via the normal FET.

The Examiner maintains that Nakai teaches or suggests each feature of claims 2 an d 8. However, while Nakai describes the concept of providing ferroelectric gate transistors as memory elements, Nakai does not disclose or suggest "a drive circuit constituted by ferroelectric

gate field-effect transistors respectively connected to the pixel electrodes" such that "said driving circuit writes data to said ferroelectric gate field-effect transistors in order of a row" (claims 2 and 8). That is, nowhere does Nakai disclose or suggest that the data to the ferroelectric gate field effect transistors must be written **in order of a row**. It appears that Nakai is completely silent as to whether the data is written in order of a row, or in order of a column, in its liquid crystal display device. The burden is on the Examiner to explain with specificity how this claimed feature is disclosed by Nakai, which burden the Examiner has not met. Therefore, claims 2 and 8 are patentable for at least these reasons. Claims 3 and 9 are patentable based on their dependency. With further regard to claim 9, this claim describes a current driven light emitting layer. Nakai is silent on this point, and such ambiguities must be construed against the Examiner.

With regard to claims 4 and 10, Nakai does not disclose or suggest changing the polarization state of the ferroelectric gate of the ferroelectric gate transistor as recited therein. That is, Nakai discloses ferroelectric gate transistors which do nothing more than "hold" a selecting state (see, for example, Nakai, col. 15, lines 36-41).

With regard to claims 5 and 11, Nakai does not disclose or suggest employing a ferroelectric gate field-effect transistor to perform row selection. On the contrary, Nakai employs a "p-Si TFT, an "a-Si TFT, a "μc-Si", or a silicon-germanium alloy transistor 101 (see Fig. 1).

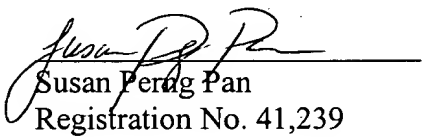
Additionally, Applicant submits that because the subject matter of claims 4-6 and 10-11 were previously before the Examiner, should an additional art rejection be applied against these claims, the rejection must be made on a non-final basis.

Furthermore, new dependent claims 12-16 are patentably distinct from Nakai at least for the reasons set forth above with respect to their respective base claims. Claims 17-27 describe features of the invention more particularly. Applicant submits that the features of the dependent claims 17-27 provide significant advantages over Nakai. For example, the use of a single FET and a single semiconductor type reduces the cost and complexity of manufacturing the light modulation device. By contrast, Nakai requires two types of semiconductor materials in fabrication. Additionally, the direct connection of the gate electrode to a selecting line as described in claim 27 eliminates the need to have an intermediate FET interconnecting the ferroelectric FET and the selection line. This also simplifies the manufacturing process.

In view of the above, Applicant submits that claims 2-6 and 8-11 and additional claims 12-27 are in condition for allowance. Therefore it is respectfully requested that the subject application be passed to issue at the earliest possible time. The Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

Applicant hereby petitions for any extension of time which may be required to maintain the pendency of this case, and any required fee, except for the Issue Fee, for such extension is to be charged to Deposit Account No. 19-4880.

Respectfully submitted,



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Date: January 3, 2001